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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Akira MOCHIZUKI

Title: REGISTER FILE AND METHOD FOR DESIGNING A REGISTER FILE

Appl. No.: 10/658,202

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Examiner: Binh C. Tat

Art Unit: 2825

Confirmation Number: 3238

CORRECTED STATEMENT OF RELEVANCE AND STATEMENT FOR IDS FILED

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This corrected statement of relevance and statement is submitted to provide a corrected statement of relevance, and a corrected statement under 37 CFR §1.97(e)(1), for the documents submitted in the Information Disclosure Statement filed on October 29, 2007. The statement of relevance for the documents submitted in the Information Disclosure Statement filed on October 29, 2007 of "The relevance of the foreign-language documents is described in the specification" is incorrect. This error was inadvertent. A revised statement of relevance and statement under 37 CFR §1.97(e)(1) is provided below.

RELEVANCE OF EACH DOCUMENT

The relevance of the foreign-language documents submitted in the Information Disclosure Statement filed on October 29, 2007 are described in a Japanese Office Action dated October 1, 2007 in the corresponding counterpart Japanese application.

A translation of a portion of a Japanese Office Action that issued October 1, 2007, with respect to the counterpart Japanese patent application, is provided below.

- Claim 1
- Cited Literature 1–4
- Remarks

Cited Literature 1 describes a register bank comprising a write side selector 56W and a read side selector 56R.

Furthermore, constituting a selection circuit from a logical AND circuit and logical OR circuit and inputting a selection signal and input signal into a logical AND circuit to generate an output signal only when the input signal has been selected by the selection signal is well-known art in the field of selection circuits, as described, for instance, in Cited Example 2 (see especially Figure 1).

Applying the well-known art of selection circuits to the write side selector of Cited Example 1 to constitute the write side selector from a logical AND circuit and a logical OR circuit and create a circuit wherein the output signal of the selection circuit changes only when the write register has been selected is a matter that could have been easily conceived of by a person skilled in the art.

Performing selection control with prioritization by taking the logical sum with the inversion signal for the signal of higher priority order is well-known art in the field of selection circuits, as described, for instance, in Cited Example 3 (see especially paragraphs (0022) through (0024)) and Cited Example 4 (see especially Figure 5); when the write side

selector of Cited Example 1 is constituted as a well-known selection circuit consisting of a logical AND circuit and a logical OR circuit, taking the logical sum with the inversion signal for the selection signal is no more than a design matter that could be suitably accomplished as necessary by a person skilled in the art, for instance, if one wanted to perform selection control with prioritization.

- Claim 2
- Cited Literature 1–4
- Remarks

Applying the well-known art of selection circuits to the read side selector of Cited Example 1 to constitute the read side selector from a logical AND circuit and a logical OR circuit is a matter that could have been easily conceived of by a person skilled in the art.

- Claim 3
- Cited Literature 1–5
- Remarks

A synchronous D-type flip-flop having a master latch and a slave latch is well known, as described, for instance, in Cited Example 5, and no remarkable difficulty is found in employing a well-known D-type flip-flop for a register.

- Claim 4
- Cited Literature 1–7
- Remarks

Generating a write signal based on decoder output and a write permission signal, as described, for instance, in Cited Example 6 (see especially Figure 1 and Figure 3) and Cited Example 7 (see especially page 804, Figure B.20), does not go beyond the well-known art.

- Claim 5
- Cited Literature 1–2

Cited Example 1 describes a register bank comprising a read side selector 56R.

Furthermore, constituting a selection circuit from a logical AND circuit and logical OR circuit and inputting a selection signal and input signal into a logical AND circuit to generate an output signal only when the input signal has been selected by the selection signal is well-known art in the field of selection circuits, as described, for instance, in Cited Example 2 (see especially Figure 1).

Applying the well-known art of selection circuits to the read side selector of Cited Example 1 to constitute the read side selector from a logical AND circuit and a logical OR circuit is a matter that could have been easily conceived of by a person skilled in the art.

- Claim 6
- Cited Literature 1–2

Describing circuits using a hardware description language is well-known art in the field of circuit design, and the question of what hardware language to use for the description is a design matter that could be suitably determined by a person skilled in the art according to the target circuit to be designed.

If any reasons for rejection are newly discovered, a notification of reasons for rejection will be issued.

List of Cited Literature

1. Japanese Unexamined Patent Application Publication H02–277125
2. Japanese Unexamined Patent Application Publication H07–038398
3. Japanese Unexamined Patent Application Publication H10–275075
4. Japanese Unexamined Patent Application Publication S59–106021
5. Japanese Unexamined Patent Application Publication H05–206791
6. Japanese Unexamined Patent Application Publication H07–262003
7. John L. Hennessy, B.5 Memory Elements, Computer Organization and Design, 2nd Edition (Volume 2), Japan, Nikkei Business Publications, Inc., Hisashi Okamura, May 17, 1999, 2nd Edition, pp. 799–804

Applicant's statement regarding the Japanese Office Action is based on a partial translation that Applicant's representative obtained. These statements should in no way be considered as an agreement by Applicant with, or an admission of, what is asserted in the Japanese Office Action.

Applicant respectfully requests that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

STATEMENT

The undersigned hereby states in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this supplemental information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to filing of this Statement.

FEE

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date November 14, 2007 By _____

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